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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,030	09/26/2001	Partha P. Datta Ray	L13.12-0117/99-369	9897

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,030	DATTA RAY ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-28* is/are allowed.

6)☒ Claim(s) *1,2,11 and 12* is/are rejected.

7)☒ Claim(s) *3-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicants' amendment filed on 04/14/2005. Claims 1-28 are pending in the action.

Drawings

Applicants' formal replacement drawings, submitted on 04/15/2005, are acceptable for examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, and 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Lembach et al, US patent no. 4,698,760.

As per claim 1, Lembach anticipates a block based design methodology with design feature limitation very identical to the claimed invention. According to Lembach, the method of optimizing functional block within a netlist of an integrated circuit design, the method comprising:

assigning corresponding delay value to each a plurality of pins the block, wherein each pin corresponds respective signal path through the block and wherein the delay values together form a delay value combination that selected from continuous set of possible combinations which each combination in the set satisfies predetermined criteria (cols. 5-6);

and generating a circuit configuration for the block with plurality logic cells are interconnected the netlist that the respective signal paths through block have delays based the corresponding delay values assigned step (cols. 4, lines 23-42, col. 5, line 11 to col. 7, line 16, col. 11, line 67 to col. 12, line 38, col. 13, line 25 to col. 14, line 23).

As per claim 2, Lembach anticipates each the logic cell has an estimated base delay Di each delay value in the delay value combination above satisfies first inequality such as delay bound as claimed (col. 4, line 43 to col. 9, line 5), and other inequality as claimed due to delay in signal propagation.

As per claim 11, Lembach anticipates functional blocks comprising logic blocks having multiple inputs with logical connection and property as claimed (Figs. 1, 3).

As per claim 12, Lembach anticipates fanout and distribution blocks to fanout, signal paths, multiple outputs, block pins, etc. (cols. 5-8).

Allowable Subject Matter

1. Claims 3-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-10 further require steps:

Assigning a corresponding delay value to each of the plurality of pins of each of the plurality of functional blocks based on the current penalty value for that pin,

Identifying critical pin in the netlist,

Updating the current penalty value of the at least one critical pin based on a history of that pin,

Repeating the step of assigning penalty function using the current penalty value for update.

Because Lembach does not expressly disclose or suggest the steps above, dependent claims 3-10 are objected to, but would be allowable if rewritten in independent form including all the limitations of base claims and any intervening claims.

2. Claims 13-28 are allowed. The following is a statement of reasons for the indication of allowable subject matter:

Claims 13-28 are directed to a method and system for adaptively timing and optimizing functional block timing within a netlist of an integrated circuit design The claims require steps and means:

Assigning a corresponding delay value to each of the plurality of pins of each of the plurality of functional blocks based on the current penalty value for that pin,

Identifying critical pin in the netlist,

Updating the current penalty value of the at least one critical pin based on a history of that pin,

Repeating the step of assigning penalty function using the current penalty value for update.

Because Lembach does not expressly disclose or suggest the steps above, claims 13-28 are thus deemed allowable.

Response to Arguments

Applicant's arguments filed 04/14 /2005 have been fully considered but they are not persuasive.

In response to applicants' argument Lembach does not disclose or suggest "generating a circuit configuration for the block with a plurality of logic cells that are interconnected in the netlist such that the respective signal paths through the block have delays based on the corresponding delay values assigned in step (a) (page 5, last two paragraphs),the examiner disagrees with. Lembach discloses a method and design apparatus for designing integrated circuits with a plurality of logic blocks (Figs. 1 and 4). The design method includes the argued feature above namely the design logic blocks are interconnected in the netlist (col. 4, lines 23-35) such that the respective signal paths (Figs. 1 and 4) between and through logic blocks having delay values based on the corresponding delay as assigned, imposed or desired to meet the design specification (Fig. 4, "Determine time delay for each and all logic blocks along interconnection paths", col. 14, lines 4-5). Lembach also discloses final design with the specified design configuration such as power configuration is generated (col. 4, lines 23-42, col. 6, lines 37-46, col. 11, for example). Lembach also discloses certain logic

designs changes should be made to meet timing requirement. Such design changes would include change of technologies, design modification, logic circuit design changes, etc. as shown above. It's clear from Lembach in order to meet timing requirement, circuit power configuration data, logic design technology, design configurations, and other design methodologies would be taken to improve design performance and meet the specification requirement.

In response to applicants' argument Lembach does not disclose assigning delay values together form a delay value combination that is selected from a continuous set of possible combinations in which each combination in the set satisfies a predetermined criteria (pages 5 and 6), the examiner disagrees with. Lembach discloses a step of assigning or predetermining delay values for each interconnected blocks and block combinations together forming a delay combinations in which each delay combination for interconnection paths satisfies a predetermined timing criteria (col. 6, line 37 to col. 8, line 15, cols. 11-14).

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 4,924,430, issued to Zasio et al, on May 1990
2. US patent o. 5,508,937, issued to Abato et al, on Apr. 1996
3. US patent no. 5,521,837, issued to Frankle et al, on May 1996
4. US patent no. 5,983,008, issued to Kumashiro et al, on Nov. 1999
5. US patent no. 6,763,506 B1, issued to Betz et al, on July 2004

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 571-272-3783. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 20, 2005

Thai Phan
Patent Examiner